INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

OIPE JC117 MAY 2 8 2002 PATENT & TRADEMARK OFFICE
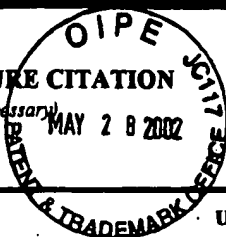
Docket Number (Optional)	Application Number
BUR920010192US1	10/063427

Applicant(s)
Mitchell DeHond, et al.

Filing Date	Group Art Unit
04/23/02	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
BB		3,751,647	08/07/73	Maeder, et al.			
BB		5,084,824	01/28/92	Lam, et al.			
BB		5,438,527	08/01/95	Feldbaumer, et al.			
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BB		6,210,983	04/03/01	Atchison, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	NO
BB		JP6216249	08/05/94	Japan				
BB		JP1024225	09/11/98	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

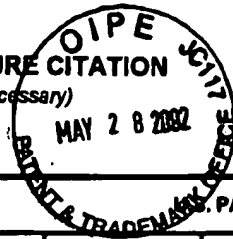|		
BB		Michael Retersdorf, "Yield Focused Defect Reduction Methodology", 3/99, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 309 - 313
BB		K.W. Lallier and A.D. Savkar, "Relating Logic Design to Physical Geometry in LSI Chip", IBM Technical Disclosure Bulletin, Vol. 19 No. 6, November 1976, pp. 2140-2143.

EXAMINER	DATE CONSIDERED
[signature]	3/5/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

F rm PT -A820
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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
BB		6,305,004	10/16/01	Tellez, et al.			
BB		6,311,139	10/30/01	Kuroda, et al.			

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BB		C.H. Stapper, "High Yield Semiconductor Logic Wiring", Vol. 30 No. 11 April 1988, IBM Technical Disclosure Bulletin, pp. 366-367.
BB		D.Guedj and M. Rivier, "Method to Computer the Random Photo Yield of Integrated Circuits", Vol. 32, No. 7, December 1989, IBM Technical Disclosure Bulletin, pp. 242 - 244.

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